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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/640,260	08/16/2000	Joseph B. Tompkins	9215/020	4626

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SETTER OLLILA, LLC
2060 BROADWAY
SUITE 300
BOULDER, CO 80302

EXAMINER	
SEFCHECK, GREGORY B	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/640,260	TOMPKINS ET AL.	
	Examiner	Art Unit	
	Gregory B Sefcheck	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-21,23-28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-21,23-28 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- Applicant's Request for Continued Examination filed 7/2/2004 is acknowledged
- Claims 1 and 18 have been amended. Claims 5, 22, and 29 have been canceled
- Claims 1-4, 6-21, 23-28, and 30-34 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6-9, 12, 13, 18-21, 23-26, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (US006504846B1), hereafter Yu, in view of Koufopavlou et al. (US005493652A), hereafter Koufopavlou.

- In regards to Claim 1, 6, 18, and 23,

Yu discloses an integrated circuit for enabling communication of data packets (Fig. 2-3C; Col. 4, lines 57-58; Col. 11, lines 60-61; claim 1,18 – method of operating an integrated circuit that processes communication packets).

Yu shows the circuit creates a plurality of buffers in external memory to store received packets. Frame pointers are used to identify the location of the stored packet (Fig. 2; Col. 6, lines 49-59; claim 1,18 – core processor configured to create plurality of

external buffers to store packets, where each buffer is associated with a pointer; claim 1,18 – pointer cache configured to store a subset of the pointers of the buffers).

Yu shows that queuing logic 74 uses a fetched frame pointer from the free buffer pool 64 to store received data to external memory 36 (Fig. 2; Col. 8, lines 28-33 and 48-62) and dequeuing logic 76 reads data from external memory, at which point the frame pointer is returned to the free buffer queue (Fig. 3, lines 27-45; claim 1,18 – control logic configured to allocate buffers as the corresponding pointers are read from the pointer cache and de-allocate the buffers as the corresponding pointers are written back to the pointer cache).

Yu does not explicitly disclose transferring an exhaustion signal if a number of pointers to de-allocated buffers reaches a minimum threshold and creating additional buffers and corresponding pointer in response to the exhaustion signal.

Koufopavlou discloses a management system for a buffer memory (Title). Referring to Figs. 1 and 2, Koufopavlou discloses maintaining a pointer memory for identifying free buffers in a buffer memory. When a new buffer is required for received data, a check is done to see if there are entries in the pointer memory. If not, a memory area (second buffer pool) of contiguous free buffers are used to store the received data and the pointer memory is updated (Col. 3, lines 15-20; Col. 4, lines 20-46; claim 1,18 – control logic transfers an exhaustion signal if a number of pointers to the de-allocated buffers reaches a minimum threshold; claim 1,18 – core processor creates additional

buffers and corresponding pointers in response to exhaustion signal; claim 6,23 – buffers distributed among at least two pools).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Yu by utilizing an area of contiguous free buffers when the number of free buffers in pointer memory are exhausted, as taught by Koufopavlou. This modification would provide a reserve pool of free memory locations to be used when the other areas of memory have been exhausted. Reserving these free locations in a contiguous area of memory reduces the number of free pointers required, thereby reducing the total memory space needed.

- In regards to Claims 2 and 19,

Yu in view of Koufopavlou discloses an integrated circuit for enabling communication of data packets that covers all limitations of the parent claims.

Yu shows that the use of a free buffer queue 64 tracks frame pointers that are available for allocation to received data and/or have been de-allocated from memory when data is transmitted (Fig. 2; Col. 9, lines 43-60; claim 2,19 – control logic tracks a number of the pointer to the de-allocated buffers).

- In regards to Claims 3 and 20,

Yu in view of Koufopavlou discloses an integrated circuit for enabling communication of data packets that covers all limitations of the parent claims.

Yu shows the ordering of the frame pointers input to the reclaim queue write side 612 may be maintained such that when space clears in the reclaim queue read side, frame pointers are moved from the reclaim queue overflow area to the reclaim queue read side (Col. 14, lines 13-17; claim 3,20 – control logic transfers additional pointers to the pointer cache if a number of the pointers to the de-allocated buffers reaches a minimum threshold).

- In regards to Claims 4 and 21,

Yu in view of Koufopavlou discloses an integrated circuit for enabling communication of data packets that covers all limitations of the parent claims.

Yu shows that additional frame pointers written to the reclaim queue write side when the reclaim queue read side is full are placed into the reclaim queue overflow (Col. 13-14, lines 65-3; claim 4,21 – control logic transfers an excess portion of the pointers from the cache if the number of pointers to de-allocated buffers reaches a maximum threshold).

- In regards to Claims 7-9, 12, 13, 24-26, and 30,

Yu in view of Koufopavlou discloses an integrated circuit for enabling communication of data packets that covers all limitations of the parent claims.

Referring to Fig. 2, Yu discloses that each of the output queues 58 and the associated frame pointers have a high and low priority queue for high and low priority frames and the associated frame pointers (Col. 9, lines 19-22; claim 7,24 – buffers and pointers are distributed among a plurality of classes; claim 8,25 – control logic tracks a number of the pointers to de-allocated buffers for at least one of the classes; claim 9,26 – control logic tracks a number of the pointers to allocated buffers for at least one of the classes; claim 12 – control logic transfers an exhaustion signal if a number of the pointers to de-allocated buffers in one of the classes reaches a minimum value; claim 13,30 – control logic tracks a number of the pointer distributed to one of the classes).

3. Claims 10, 11, 14-17, 27, 28, and 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Koufopavlou as applied to claims 7 and 24 above, and further in view of Janoska et al. (US006539024B1), hereafter Janoska.

- In regards to Claims 10, 11, 27, and 28,

Yu in view of Koufopavlou discloses an integrated circuit for enabling communication of data packets that covers all limitations of the parent claims.

Yu does not explicitly show at least some of the pointers from a first class being borrowed for use by a second class.

Referring to Fig. 5, Janoska further shows that a shared memory portion used by all logical queues (Col. 6, lines 21-37; claim 10,27 – control logic borrows at least some of the pointers from a first one of the classes for use by a second one of the classes; claim 11,28 – control logic redistributes some of the pointers from a first class to a second class).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Yu by allowing pointers to be shared amongst multiple classes of data queue, thereby encouraging more efficient use of available buffering resources, as taught by Janoska.

- In regards to Claims 14-17 and 31-34,

Yu in view of Koufopavlou discloses an integrated circuit for enabling communication of data packets that covers all limitations of the parent claims.

Yu does not explicitly disclose distributing pointers among classes where at least one of the classes is associated only with constant bit rate packets, one only with available bit rate packets, one only with variable bit rate packets and one only with unspecified bit rate packets.

Janoska discloses data buffer management in a communications switch. Janoska shows that received data cells are put into different classes based on their type of service in the network (Col. 3, lines 54-61; claim 14,31 – at least one of the classes is associated only with constant bit rate packets; claim 15,32 – at least one of the classes is associated only with available bit rate packets; claim 16,33 – at least one of the

classes is associated only with variable bit rate packets; claim 17,34 – at least one of the classes is associated only with unspecified bit rate packets).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Yu for distributing pointer among classes for each of a different type traffic stream, such as CBR, VBR, ABR and UBR, as taught by Janoska, thus enabling managing the different quality of service provided to each traffic type.

Response to Arguments

4. Applicant's arguments with respect to claims 1-4, 6-21, 23-28, and 30-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Kao (US 20030037096A1) discloses a method and apparatus for the management of queue pointers by multiple processors in a digital communications network
- Hostetter (US 20020004894A1) discloses a pointer verification system and method
- Roy et al. (US006246682B1) discloses a method and apparatus for managing multiple ATM cell queues

- Sorber (US006088777A) discloses a memory system and method for dynamically allocating a memory divided into plural classes with different block sizes to store variable length messages
- Hasegawa et al. (US006046983A) discloses a dynamic rate control system
- Badger et al. (US005606559A) discloses a system and method for an efficient ATM adapter/device driver interface

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory B Sefcheck whose telephone number is 571-272-3098. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GBS
2-1-2005

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600